DIGITAL VIDEO BROADCASTING SATELLITE RECEIVER BASED ON HIGH PERFORMANCE SINGLE CHIP MICROPROCESSOR

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This paper discusses new technologies in communication systems and particularly the new systems for transmitting audio and video data, which switch from analog to digital principle. The number of digital channels transmitted through satellites increased every day. The trend in the near future is for replacement all the analogue TV and Radio broadcasting with digital one. To unify the implementation of dynamic interactive systems, middleware kernels will be built-in in such systems, as some of these kernels are Open TV and MHP allowing integration of Java virtual machine, TCP/IP stack, browser and etc.

Keywords: Digital Video Broadcasting, set-top-box, ST5518, MPEG-2

1.INTRODUCTION

DVB project is starting in September 1993, like organization compound of private and national company which is engaged in TV broadcasting. DVB create the frame of MPEG-2 based digital video service. Before starting of this new phase of using digital method for compressing and transmitting data, there were used analog methods. Frequency modulation for video channel and double frequency modulation for audio channel is used in the analogue satellite transmission [2]. The advantages of the digital television over the analog are:

- Higher noise stability, better quality, only two signals are transmitted: 1 and 0
- Ability for more programs to be transmitted in the same frequency band
- Easiest ways for coding.
- Ability of error correction.
- Ability of transmitting much additional information - EPG, teletext, subtitles, languages, additional information, etc.
- Ability of integrating PVR (Personal Video Recording) on hard disk drive directly from the transport stream.

2.CPU OVERVIEW

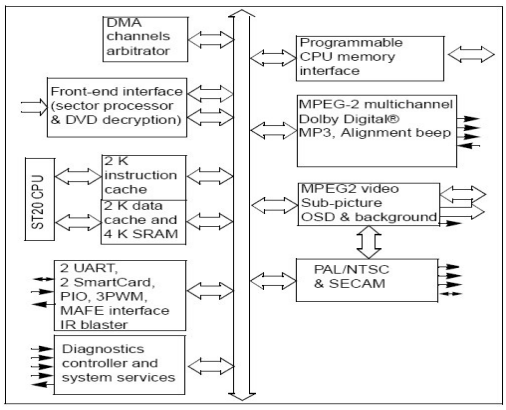
STi5518 [6] is high integrating single-chip decoder, design for use in feature rich mass-marked set-top boxes. It integrates high-performance 32-bits CPU, separated block for DVB/DirecTV transport de-multiplexing and de-scrambling, modules for MPEG-2 video and audio decoding with 3D-surround and MP3 support, advanced display and graphics features and digital video encoder.

The STi5518 Central Processing Unit (CPU) is a ST20C2+ 32-bit processor core. It contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the high-speed on-chip SRAM, which can store data or programs and uses the cache to reduce access time to off-chip program and data memory. MPEG video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards. User-defined bitmaps can be super-imposed on the display picture by using the on-screen display function. The display unit is part of the MPEG video decoder, it overlays the four display planes - background color, MPEG video, on-screen display and sub-picture plane. The audio decoder accepts: Dolby Digital [7], MPEG-1 layers I, II and III, MPEG-2 layer II 6-channel, PCM, CDDA data formats; MPEG2 PES streams for MPEG-2, MPEG-1, Dolby Digital [7], MP3, and Linear PCM (LPCM). The audio decoder supports DTS® digital out (DVD DTS and CDDA DTS). Sampling frequencies of 96 kHz, 48 kHz, 44.1 kHz, 32 kHz and half sampling frequencies are supported. CPU has integrated S-PDIF digital audio output. The digital signal is coded using the 'bi phase-mark-code' (BMC), which is a kind of phase modulation. So you can use a low-cost software state machine decoder to obtain digital data [3].

The STi5518 provides a pulse-position modulated signal for automatic VCR programming by the set-top box. The signal is output to the IR blast pin and an accessory jack pin, simultaneously. The Modem Analogue Front-End interface is used to transfer transmit and receive DAC and ADC samples between the memory and an external modem analogue front-end (MAFE), using a synchronous serial protocol.

The on-chip memory includes 2 Kbytes of instruction cache, 2 Kbytes of data cache and 4 Kbytes of SRAM that can be optionally configured as data cache. The sub-system provides 240 Mbytes/s of internal bandwidth, supporting pipelined 2-cycle internal memory access. The instruction and data caches are direct-mapped, with a write-back system for the data-cache. The caches support burst accesses to the external memories for refill and write-back. Burst access increases the performance of page mode DRAM memories.

There are two off-chip memory interfaces: External memory interface (EMI) accessed by the ST20 is used for the transfer of data and programs between the STi5518 and external peripherals, flash and additional SDRAM and DRAM. Shared memory interface (SMI) controls the movement of data between the STi5518 and 16, 32 or 64Mbits of SDRAM. This external SDRAM stores the display data generated by the MPEG decoder and CPU and the C2+ code data.



The Asynchronous Serial Controller (ASC), also referred to as the UART interface, provides serial communication between the STi5518 and other microcontrollers, microprocessors or external peripherals. The STi5518 has four ASCs, two of which are generally used by the SmartCard controllers. Two synchronous serial controllers (SSC) provide high-speed interfaces to a wide variety of serial memories, remote control receivers and other microcontrollers. The SSCs support all of the features of the serial peripheral interface bus (SPI) and the I2C bus.

The on-chip PLL accepts 27 MHz input and generates all the internal high-frequency clocks needed for the CPU, MPEG and audio sub-systems.

The ST20 diagnostic controller unit (DCU) is used to boot the CPU and to control and monitor the chip systems.

The interrupt system allows an on-chip module or external interrupt pin to interrupt an active process so that an interrupt handling process can be run.

The integrated digital encoder converts a multiplexed 4:2:2 or 4:4:4 YCbCr stream into a standard analog baseband PAL/NTSC or SECAM signal and into RGB, YUV, Yc and CVBS components. The encoder can perform closed-caption, CGMS encoding, and allows Macrovision^{TM} 7.01/6.1 copy protection.

3. STB PROTOTYPE DESIGN:

On Fig. 2 is presented block diagram of integrated receiver decoder for digital satellite television, developed by R&D division of Valvecs Holding PLC [8]. The design includes CPU (central processor unit), responsible for management the interfaces and processing MPEG-2 data.

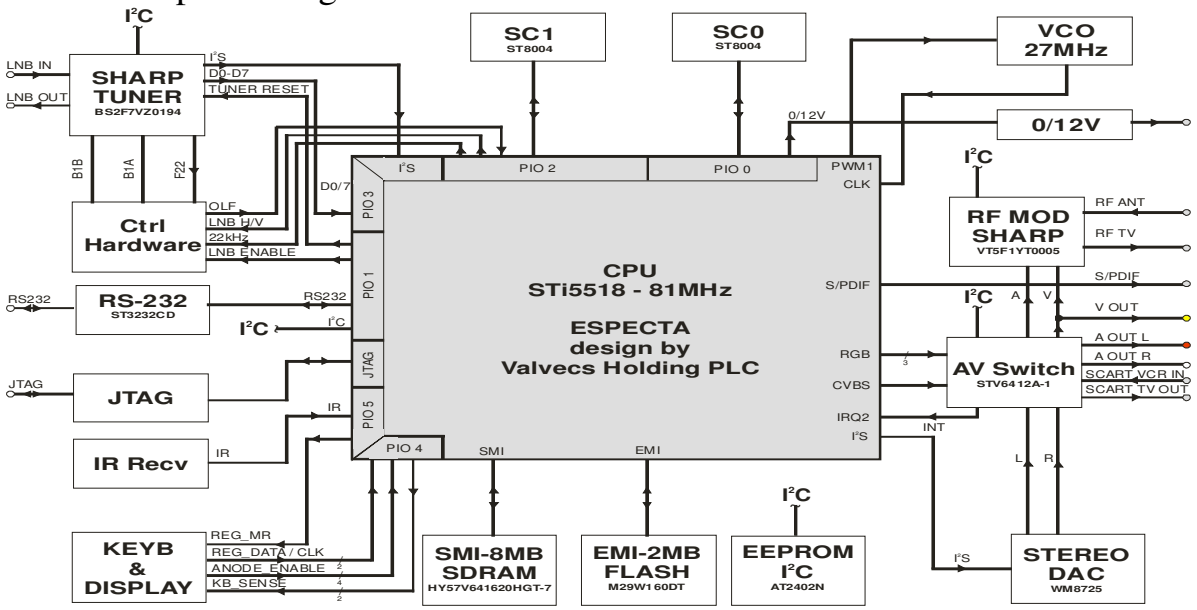


Fig. 2 – Prototype design

Tuner – controlled by I2C bus for selecting frequency on which to lock, setting the polarizations, selecting low or high KU band, QSPK demodulator, 8-bit data bus, loop-trough for redirecting input signal to next device.

RS-232 asynchronous serial interface is used for updating the firmware or connecting whit another IRD. JTAG interface is used for in circuit programming and debugging. Keyboard and display is used for controlling the IRD and displaying information about selected channel, time or any kind of service information. IR receiver accepts signals form remote control.

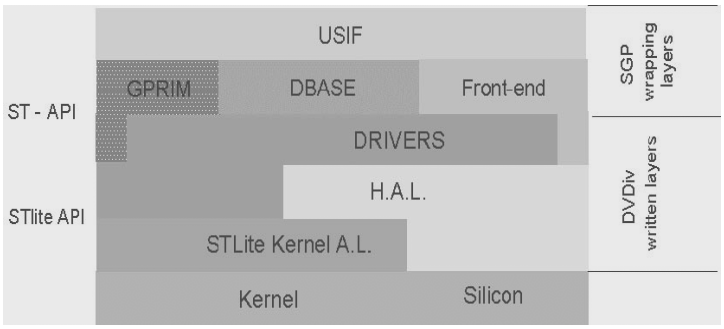
SDRAM is the place where, at switching on the CPU the whole program is copied and executed, also a place for audio and video data temporary storage. FLASH memory is the place, where the software of the receiver is copied and saved. EEPROM memory is the place where data for factory reset is recorded (permanent - without any changes) and also information for the current state of the intensity of the sound, the selected program number, timer activated etc.

Stereo DAC is WM8725 [9], supporting frequency sampling from 8 KHz to 96 KHz and resolution to 24bit via normal or I2S serial data interfaces. Information for sound symbols is passed to DAC and it converts the audio data in analog type and then this signal is transmitted to AV Switch.

STV6412A [6] is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. The RF Modulator used in this design is RMUP74055 [10]. It has input for connecting external antenna for terrestrial broadcasted channels, RF output with channel between 21-69, TV system broadcast method PAL-G /I /K/ M and selectable audio carrier frequency of 4.5/ 5.5/ 6.0/ 6.5MHz as selecting channels and all other parameters is executed by I²C bus.

4. SOFTWARE STACK (libaries, drivers):

The operating system is OS20 [6], which is RTOS. The programming language is ANSI C and there is a specialized optimized compiler. A structure of the software model is shown on Fig. 3. USIF - User Interface is the highest level of software architecture, which represents a graphic console with which the user works. The following is managed by this console: Dbase – Data Base, Front End Tuner, GPRIM Drivers, H.A.L – hardware application layer, Kernel Silicon – hardware on which the whole receiver is constructed, ST-Lite Real Time Operating System.



Software Architecture is based on API witch is fully documented that minimizes development times. This API is designed such a way that the hardware changes are "invisible" and the drivers keep their internal consistency. ST API [6] is well appropriate for several "middlewares" and allows developers to build layers on top. Adaptation layers for popular middlewares such as OpenTV [4], MediaHighway are available.

5. CONDITIONAL ACCESS:

Many of TV channels are encrypted to prevent illegal access to their contents. There are two methods for descrambling service. First is embedded conditional access system. ST5518 has two smart card interfaces for connecting external card readers, and possibility for integrating embedded Conditional Access system. Embedded CA is responsible for transmitting special type of messages from transport stream to the card, which it uses to generate key for decrypting the channel.

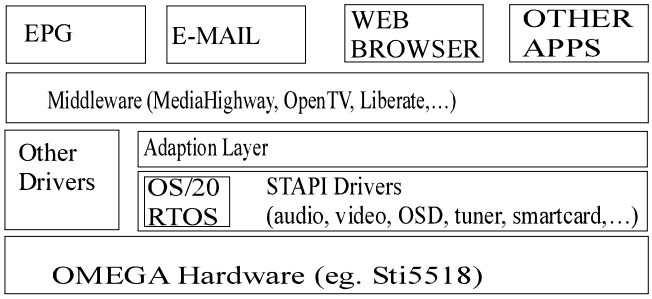
The second way is to use Common Interface. This interface is used to enable a CA module (Conditional Access-Module) to be used with the DVB receiver. This module is connecting between tuner and CPU by common interface hardware controller. STV0700 [6] is dual common interface hardware controller, which allows two PCMCIA card to be connected. These PCMCIA modules are used to descrambling the transport stream.

6. MIDDLEWARE:

There are several middleware some of them are OpenTv [4], MHP [5], MediaHighway. The Multimedia Home Platform (MHP) [5] defines a generic interface between interactive digital applications and the terminals on which those applications execute. It enables digital content providers to address all types of terminals ranging from low-end to high-end set top boxes, integrated digital TV sets and multimedia PCs. The MHP extends the existing, successful DVB open standards for broadcast and interactive services in all transmission networks. ETSI TS102 812 is the technical specification for the MHP middleware. The MHP model considers 3 layers: ***resources, system software*** and ***applications***. The API lies between the *Applications* and *System software* seen from the perspective of an application.

The hardware entities in the platform include a number of functions. Hardware or software resources represent them. There is no assumption about how they are grouped. The model considers that there can be more than one hardware entity in the total Platform. From an abstract point of view it makes no difference if the logical resources are mapped into one or several hardware entities. What is important is that resources are provided to the MHP transparently. An application should be able to access all locally connected resources as if they were elements of a single entity.

Applications will not directly address resources. The system software brings an abstract view of such resources. This middle layer isolates the application from the hardware, enabling portability of the application. The system software includes an application management function, which is responsible for managing the lifecycle of all applications, including Interoperable ones. Applications implement interactive services as software running in one or more hardware entities. The interface for MHP applications is a top view from application to the system software.



7. CONCLUSIONS AND FUTURE WORK

The trend is to replace all analogue TV and Radio broadcasting systems with digital one. In this publication we presented a low-cost digital receiver reviewing all the basic modules of one digital receiver. Digital technology provides more efficient bandwidth management. That will allow transmitting more TV and radio channels on the same bandwidth. Here we review typical satellite receiver but future experiments will be focused on cable digital receivers also terrestrial ones, investigation of IP-TV and integration of middlewares. The most attractive conception indisputably is digital terrestrial broadcasting, which will be the future standard for TV broadcasting. Radio spectrum is limited so the efficiency is the most important in terrestrial broadcasting. On a standard one channel analogue bandwidth of 8MHz we can transmit up to 4 digital TV programmes with stereo sound and additional information or 3 TV channels with integration of conditional access system [1].

Digital technology offers flexibility to the cable operators in accounting and managing different programming packages. Digital technology over cable has the ability for conditional access thus the operator can easily control the status (enabled or disabled) of its users, without additional hardware changes in the cable network (mechanical disconnecting the users from the trunk-line splitters).

Digital technology also offers interactive services based on return channel to the operator. "Pay on Demand" and "Pay per View" are very popular in digital IP-TV (TV over Internet Protocol). Interactive services are based on client-server model. Thus allow to the operator to make voting systems, entertainment and chat systems, local systems for salutation etc.

Middleware cores come rapidly. Middlewares allow to the operator to support interactive functions of the whole system supporting different type of terminals (hardware in the STB). The middleware acts like virtual STB. Every virtual STB has the same commands and control. This allows running and loading of executable code over STB directly from the transport stream and thus presents the STB as a dynamic system different from the traditional static systems.

8. REFERENCES

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